Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-11 (canceled).

Claim 12. (new) A field effect transistor comprising:

a substrate having a doping of a first conductivity type;

a drain area in the substrate having a doping of a second conductivity type opposite to the first conductivity type;

a source area in the substrate being laterally spaced from the drain area and having a doping of the second conductivity type;

a channel area in the substrate disposed between the source area and the drain area; and

an area having a doping of the second conductivity type, the area connected to the drain area and arranged in a portion of the substrate adjacent to the drain area such that alternating regions having the first conductivity type and having the second conductivity type are disposed in the portion.

Claim 13. (new) The field effect transistor of claim 12, wherein the area is configured such that the portion of the substrate bordering the drain area is substantially depleted responsive to application of a predetermined drain voltage.

Claim 14. (new) The field effect transistor of claim 12, wherein the area comprises a comb-shaped cross section.

Claim 15. (new) The field effect transistor of claim 12, wherein the substrate comprises a surface at which the source area, the channel area, and the drain area are arranged, and wherein the area comprises a plurality of parallel columns extending in a direction substantially perpendicular to the surface of the substrate.

Claim 16. (new) The field effect transistor of claim 12, wherein the substrate comprises a surface at which the source area, the channel area, and the drain area are disposed, the drain area including a first side disposed near the surface and an opposing second side disposed within the substrate, and wherein the area is disposed adjacent the second side of the drain area.

Claim 17. (new) The field effect transistor of claim 12, wherein:

the substrate comprises a base substrate having a surface and an epitaxial layer epitaxially grown on the surface of the base substrate;

the source area, the drain area, and the channel area are disposed in the epitaxial layer; and

the portion in which the area is arranged extends from the drain area towards the surface of the base substrate.

Claim 18. (new) The field effect transistor of claim 12, wherein the drain area includes a low-doped drain sub-area having a plurality of drain portions in which a doping concentration in a direction toward the channel area decreases.

Claim 19. (new) The field effect transistor of claim 18, wherein a lateral dimension of the area is at least as great as a lateral dimension of a most highly doped portion of the plurality of drain portions.

Claim 20. (new) A method for use in constructing a field effect transistor, comprising:

a) forming a drain area in a substrate having a doping of a second conductivity type opposite to the first conductivity type, the substrate having a doping of the first conductivity type;

b) forming a source area in the substrate being laterally spaced from the drain area and having a doping of the second conductivity type;

c) forming a channel area in the substrate disposed between the source area and the drain area; and

d) forming an area having a doping of the second conductivity type and connected to the drain area and arranged in a portion of the substrate adjacent to the drain area such that alternating regions having the first conductivity type and having the second conductivity type are disposed in the portion.

Claim 21. (new) The method of claim 20, wherein step d) further comprises forming the area using successive epitaxy and implantation.

Claim 22. (new) The method of claim 20, wherein step b) further comprises forming the source area using lateral diffusion.

Claim 23. (new) A field effect transistor comprising:

a substrate having a first conductivity type;

a drain area in the substrate having a second conductivity type opposite to the first conductivity type;

a source area in the substrate laterally spaced from the drain area and having a doping of the second conductivity type;

a channel area in the substrate disposed between the source area and the drain area; and

a plurality of regions of the second conductivity type extending from the drain area into a portion of the substrate having the first conductivity type.

Claim 24. (new) The field effect transistor of claim 23 wherein the plurality of regions and the portion of the substrate form alternating regions having the first conductivity type and having the second conductivity type.

Claim 25. (new) The field effect transistor of claim 24, wherein the plurality of regions comprise a plurality of parallel columns.

Claim 26. (new) The field effect transistor of claim 23, wherein the plurality of regions has a comb-shaped cross section.

Claim 27. (new) The field effect transistor of claim 23, wherein the substrate comprises a surface at which the source area, the channel area, and the drain area are arranged, and wherein the plurality of regions extend in a parallel manner generally away from the surface of the substrate.

Claim 28. (new) The field effect transistor of claim 23, wherein:

the substrate comprises a base substrate having a surface and an epitaxial layer epitaxially grown on the surface of the base substrate;

the source area, the drain area, and the channel area are disposed in the epitaxial layer; and

the plurality of regions extend from the drain area towards the surface of the base substrate.

Claim 29. (new) The field effect transistor of claim 23, wherein the drain area includes a low-doped drain sub-area having a plurality of drain portions in which a doping concentration in a direction toward the channel area decreases.

Claim 30. (new) The field effect transistor of claim 29, wherein a lateral dimension of the plurality of regions is at least as great as a lateral dimension of a most highly doped portion of the plurality of drain portions.

Claim 31. (new) The field effect transistor of claim 29, wherein low-doped drain sub-area includes three laterally adjacent drain portions.